Election/Restriction

The Examiner has made FINAL within this application a restriction requirement under which applicant previously elected with traverse prosecution of Group I, claims 1-8.

In response solely to the restriction requirement made FINAL, applicant has canceled herein claims 9-15 as being drawn to an invention non-elected under the restriction requirement made FINAL.

Claim Rejections - 35 U.S.C. § 102

The Examiner has rejected claims 1-8 under 35 U.S.C. § 102(b) as being anticipated by Ashby et al. ("High *Q* Inductors for Wireless Applications in a Complementary Silicon Bipolar Process," IEEE J. of Solid-State Circuits, Vol. 11(1), Jan. 1996, pp. 4-9; hereinafter "Ashby").

Applicant respectfully disagrees with the Examiner's reading of Ashby, to the extent that the Examiner asserts that paragraph III of Ahsby's disclosure anticipates applicant's invention.

In that regard, applicant in a first instance notes that Ahsby, paragraph III, lines 4-8, clearly discloses a single spacing of 4 um between metal traces (i.e., a successive series of spirals) within each of Ashby's series of sixteen inductor structures within Ashby's test array of inductor structures.

Similarly, in a second instance, applicant understands Ashby, paragraph III, lines 8-10 to state with respect to Ashby's test array of sixteen inductor structures that "[five groups of t]hree inductors [each were fabricated] with a varying number of turns [for each of the five groups of three inductors, and] were made with [separate single width] metal trace widths [selected from the group consisting] of 5, 9, 14, 19 and 24 um, and one inductor was made with a trace width of 49 um."

Applicant believes that the above reading of Ashby is consistent with Ashby's requirement of fabricating sixteen inductor structures comprising a group of fifteen inductor structures plus one inductor structure. Applicant does not believe that there exists a reading of Ashby, paragraph III which provides for: (1) variation of a metal trace width (i.e., a successive series of spirals) within a single inductor structure; (2) formation of sixteen inductor structures in the groups of fifteen inductor structures plus one inductor structure; and (3) a varying number of turns within the five groups of three inductor structures, as is inherently or implicitly, if not explicitly, required within Ashby. Thus, applicant asserts that it is inherent or implicit, if not explicit, within Ashby that Ahsby did not vary a metal trace width (i.e., a successive series of spirals) within an individual one of Ashby's sixteen inductor structures, as is in part required within applicant's method for forming applicant's inductor structure as disclosed and claimed within claim 1.

Thus, since each and every limitation within applicant's invention as disclosed and claimed within claim 1 is not disclosed within Ashby, applicant asserts that claim 1 may not properly be rejected under 35 U.S.C. § 102(b) as being anticipated by Ashby.

Since all remaining claims within this application are dependent upon claim 1 and carry all of the limitations of claim 1, applicant additionally asserts that those remaining claims may also not properly be rejected under 35 U.S.C. § 102(b) as being anticipated by Ahsby.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of applicant's claims 1-8 under 35 U.S.C. § 102(b) as being anticipated by Ashby be withdrawn.

Other Considerations

The Examiner has cited no additional prior art of record not employed in rejecting applicant's claims to applicant's invention.

No fee is due as a result of this amendment and response.

SUMMARY

Applicant's invention as disclosed and claimed within amended claim 1 is directed towards a method for fabricating an inductor structure comprising a planar spiral conductor layer, wherein a successive series of spirals within the planar spiral conductor layer is formed with a variation in at least one of: (1) a series of linewidths of the successive series of spirals; and (2) a series of spacings separating the successive series of spirals. Absent from the

prior art of record employed in rejecting applicant's claims to applicant's invention is a disclosure or each and every limitation within applicant's invention as disclosed and claimed within claim 1.

CONCLUSION

On the basis of the above amendments and remarks, reconsideration of this application, and its early allowance, are respectfully requested.

Any inquiries relating to this or earlier communications pertaining to this application may be directed to the undersigned attorney at 248-540-4040.

Respectfully submitted,

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APPENDIX I

PORTION OF THE SPECIFICATION

(MARKED-UP WITH CURRENT REVISIONS)

Page 1, Cross-Reference to Related Application

CROSS-REFERENCE TO RELATED APPLICATION

This application is related to co-assigned application serial number [__/_____] 09/821,521, filed [__ _____ 2000] 29 March 2001, attorney docket number 67,200-261, titled "Planar Spiral Inductor Structure With Patterned Interconnected Bond Pad Region Integral Thereto," the disclosure and references from which related co-assigned application are incorporated herein fully by reference.

APPENDIX II

COMPLETE COPY OF THE CLAIMS

(MARKED-UP WITH CURRENT REVISIONS)

1. A method for fabricating an inductor structure comprising:

providing a substrate;

forming over the substrate a planar spiral conductor layer to form a planar spiral inductor, wherein a successive series of spirals within the planar spiral conductor layer is formed with a variation in at least one of:

a series of linewidths of the successive series of spirals; and

a series of spacings separating the successive series of spirals.

2. The method of claim 1 wherein by employing within the successive series of spirals within the planar spiral conductor layer the variation in at least one of the series of linewidths of the successive series of spirals and the series of spacings separating the successive series of spirals, the planar spiral inductor is fabricated with an enhanced Q value.

3. The method of claim 1 wherein the substrate is employed within a microelectronic fabrication selected from the group consisting of integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications.

4. The method of claim 1 wherein the successive series of spirals is formed in a shape selected from the group consisting of a triangle, a square, a rectangle, a higher order polygon, a uniform ellipse, a non-uniform ellipse and a circle.

5. The method of claim 1 wherein the planar spiral conductor layer is formed of a conductor material selected from the group consisting of non-magnetic metal, non-magnetic metal alloy, magnetic metal, magnetic metal alloy, doped polysilicon and polycide conductor materials, and laminates thereof.

6. The method of claim 1 wherein the variation in the series of linewidths of the successive series of spirals is an increasing progression of linewidth from a first spiral which defines the center of the planar spiral inductor having a comparatively narrow linewidth to a final spiral which defines the perimeter of the planar spiral inductor having a comparatively wide linewidth.

7. The method of claim 6 wherein the comparatively narrow linewidth is from about 7 to about 10 microns and the comparatively wide line width is from about 17 to about 21 microns.

8. The method of claim 1 wherein the successive series of spirals comprises from about 1 to about 8 spirals.

9. - 15. (Canceled)